What is claimed is:

1. A computer system comprising:

a system controller including a central processing unit and a memory bus controller and operating in a first interface mode;

a system memory connected with the system controller through the system bus;

a NAND flash memory for storing a system driving code, an operating system program and a user data for the computer system; and

an interface unit communicating with the system controller through the system bus in the first interface mode and communicating with the NAND flash memory in a second interface mode, the interface unit being synchronized with a clock signal generated therein in response to a predetermined command information and operating.

2. The computer system of claim 1, wherein the interface unit comprises:

a host interface unit communicating with the system controller through the system bus in the first interface mode;

a register unit for storing a configuration information about the computer system and the NAND flash memory and the command information about the NAND flash memory;

a buffer unit for storing data of the NAND flash memory;

an oscillator for generating the clock signal in response to the command information;

a state machine synchronized with the clock signal, for controlling an inner operation of the interface unit in response to the command information; and

a NAND flash interface unit synchronized with the clock signal and communicating with the NAND flash memory by the state machine in the second interface mode.

3. The computer system of claim 2, wherein the interface unit further comprises a power-up detector for applying a power sensing signal to the state machine when a power is applied.

4. The computer system of claim 2 or 3, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal, for performing an error test and correction on the data of the NAND flash memory.

5. The computer system of claim 4, wherein the state machine comprises:

a first block for controlling operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block for controlling an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block for controlling an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block for controlling an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and controlling an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

6. The computer system of claim 5, wherein the state machine further comprises:

a fifth block for controlling an operation to erase the data stored in the NAND flash memory; and

a sixth block for controlling a reset command applied to the NAND flash memory and resets of registers within the interface unit.

7. The computer system of claim 1, wherein the interface unit comprises:

a first interface unit communicating with the system controller through the system bus in the first interface mode;

a second interface unit synchronized with the clock signal and communicating with the NAND flash memory in the second interface mode;

a storage unit for storing information and data exchanged between the first and second interface units; and

a control unit synchronized with the clock signal, for controlling a transmission of the information and data between the first and second interface units.

8. The computer system of claim 7, wherein the storage unit comprises:

a register unit for storing a configuration information about the compute system and the NAND flash memory and the command information about the NAND flash memory; and

a buffer unit for storing data of the NAND flash memory.

9. The computer system of claim 7, wherein the interface unit further comprises a power-up detector for applying a power sensing signal to the state machine when a power is applied.

10. The computer system of claim 7 or 9, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal, for performing an error test and correction on the data of the NAND flash memory.

11. The computer system of claim 7, wherein the control unit comprises:

a first block for controlling operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block for controlling an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block for controlling an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block for controlling an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and controlling an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

12. The computer system of claim 11, wherein the control unit further comprises:

a fifth block for controlling an operation to erase the data stored in the NAND flash memory; and

a sixth block for controlling a reset command applied to the NAND flash memory and resets of registers within the interface unit.

13. A booting method of a computer system with a NAND flash memory, the method comprising:

a first step of copying a system bootstrap code to a buffer from the NAND flash memory in response to a power applying detecting state;

a second step of initializing the computer system according to the system bootstrap code stored in the buffer and copying an operating system code to a programmable memory from the NAND flash memory; and

a third step of executing the operating system code.

14. A method for reading out data from a NAND flash memory in a computer system with a system controller, a buffer and the NAND flash memory, the method comprising:

a first step of setting commands, addresses and pages to be read out to the NAND flash memory;

a second step of copying the first page data of the pages to the buffer; and

a third step of copying the second page data of the pages to the buffer from the NAND flash memory while transmitting the first page data from the buffer to the system controller.

15. The method of claim 14, wherein the third step is repeated until the data copying of the set pages is completed.

16. The method of claim 14, wherein the data of the set pages are transmitted successively.

17. A method for programming data from a NAND flash memory in a computer system with a system controller, a buffer and the NAND flash memory, the method comprising:

a first step of setting commands, addresses and pages to be programmed to the NAND flash memory;

a second step of successively loading data necessary for the pages to be programmed from the system controller to the buffer; and

a third step of sequentially executing a program for the pages by using the data loaded to the buffer.

18. The method of claim 17, wherein the program for another page is executed while the data to one page of the pages is loaded to the buffer.